ORTHOGONE Technologies Inc.

Product Brief

Rev.: 1.1

Ultra-Low Latency 10G MAC & PCS

APPLICATIONS

- High Frequency Trading
- Smart NIC
- Low-Latency Switches
- QoS-Based Packet Processing
- Test and Monitoring Equipment
- Backhaul Solution

KEY BENEFITS

- Industry leading performances
- Ultra-low gate count
- Ultra-low latency
- Ease of use
- Flexibility & scalability
- Supports wide range of FPGA devices
- High timing margin

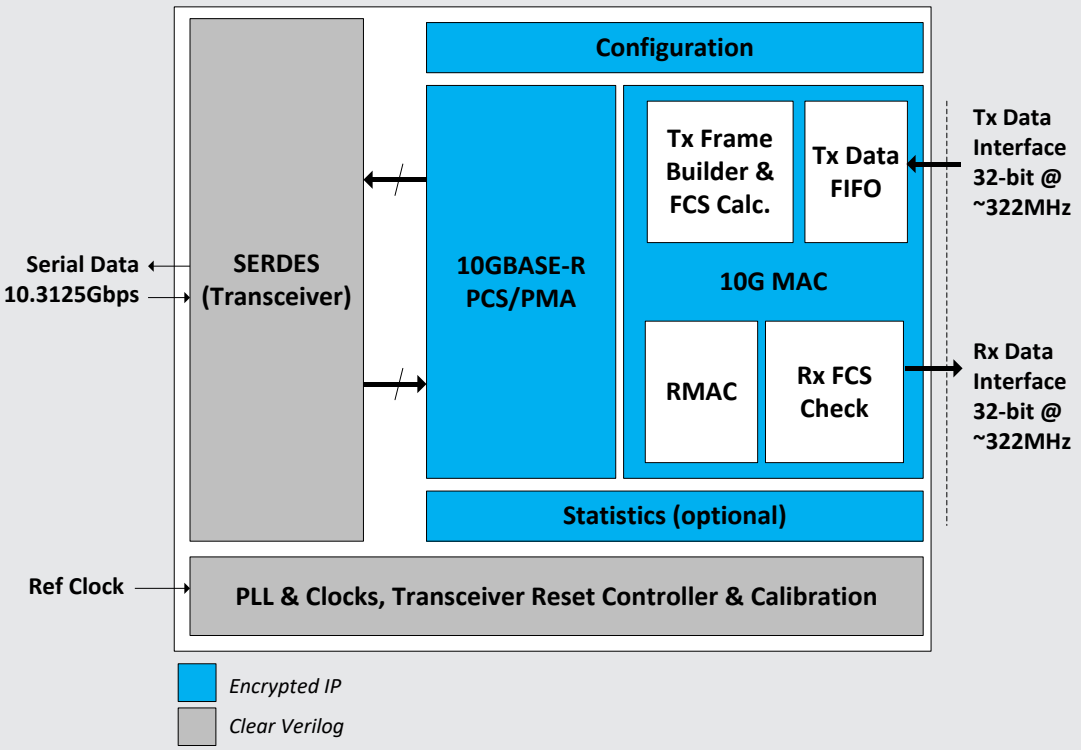
OVERVIEW

The ***Ultra-Low Latency 10G Ethernet MAC and PCS*** is the **industry leading solution** for latency critical Ethernet applications. The core is designed using **advanced design techniques** leading to unmatched ultra-low gate count utilization and amazing latency performances.

It includes a **rich set of standard and advanced features** making it ideal for a large number of applications.

The IP core can support full wire line speed with a 64-byte packet length. It also supports back-to-back or mixed length traffic, up to jumbo frame size, with no dropped packets.

HIGH-LEVEL BLOCK DIAGRAM



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DELIVERABLES

- **Datasheet & user guide**
- **Encrypted Verilog**
- **Constraints file**
- **Reference design**
- **Technical support**
- **Optional Verification IP (UVM based)**
- **Optional IP design customization**

ORDERING INFORMATION

- ***ENET-010G-L-01 (10G)***

CONTACT

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General Features

- Compliant with the IEEE 802.3-2012 High Speed Ethernet Standard
- Ethernet MAC supports 10GbE line rate with flexible feature set
- Soft PCS logic interfacing to standard serial transceiver at 10.3125Gbps
- Standard 10GbE SFI, XFI external interface operating at 10.3125Gbps

MAC Features

- Deficit idle counter (DIC) to maintain a 12-byte inter-packet gap (IPG) average
- Programmable IPG length (down to 1-byte)
- Programmable Maximum Receive Unit (MRU), Maximum Transmission Unit (MTU)
- User facing logic interface 32-bit @ 322.265625MHz
- Ethernet flow control and congestion management using pause frames with programmable quanta
- XON / XOFF Frame transmission can be triggered by host (software) interface or directly by core pause frame interface signals
- Programmable Tx minimum packet length with enable/disable padding option
- Programmable Rx minimum packet length
- Tx Frame Check Sequence (FCS) computation and insertion
- Programmable Tx FCS pass-through and corruption insertion modes
- Programmable keep/strip Rx FCS. Programmable Rx FCS error detection and marking
- Programmable Tx and Rx large frame threshold detection
- Programmable Tx and Rx path VLAN detection (Programmable TPID, stacked VLAN)
- Programmable Rx frame discard & marking
- Configurable statistics vector and collector on transmit and receive MAC data

PCS Features

- Supports 10GBASE-R PHY based on 64B/66B encoding and scrambling
- Supports block synchronization and BER monitor
- Configurable statistics vector and collector on transmit and receive PCS

Performances Overview Example

Device Family [1]	Rate [Gbps]	Resources Utilization [2]			Core clock [MHz]	Wire to Wire Round-Trip Latency [3]
		LUTs	FFs	BRAM		
UltraScale +	10-Gbps	3.31k	5.16k	0	322.265	67ns

[1] Other FPGA platforms supported: Intel PSG: Stratix-V, Arria-10, Xilinx: Series-7, UltraScale.
[2] Resources utilization includes statistics counters
[3] Latency: GTY Transceiver + PCS + MAC (Tx + Rx)