ORTHOGONE Technologies Inc.

Product Brief

Rev.: 1.0

40/100G Ethernet MAC & PCS + RS-FEC

APPLICATIONS

- Data Centers
- Smart NIC
- Low-Latency Switches
- QoS-Based Packet Processing
- Test and Monitoring Equipment
- Backhaul Solution
- Video over IP

KEY BENEFITS

- Industry leading performances
- Ultra-low gate count
- Ultra-low latency
- Ease of use
- Flexibility & scalability
- Supports wide range of FPGA devices
- High timing margin

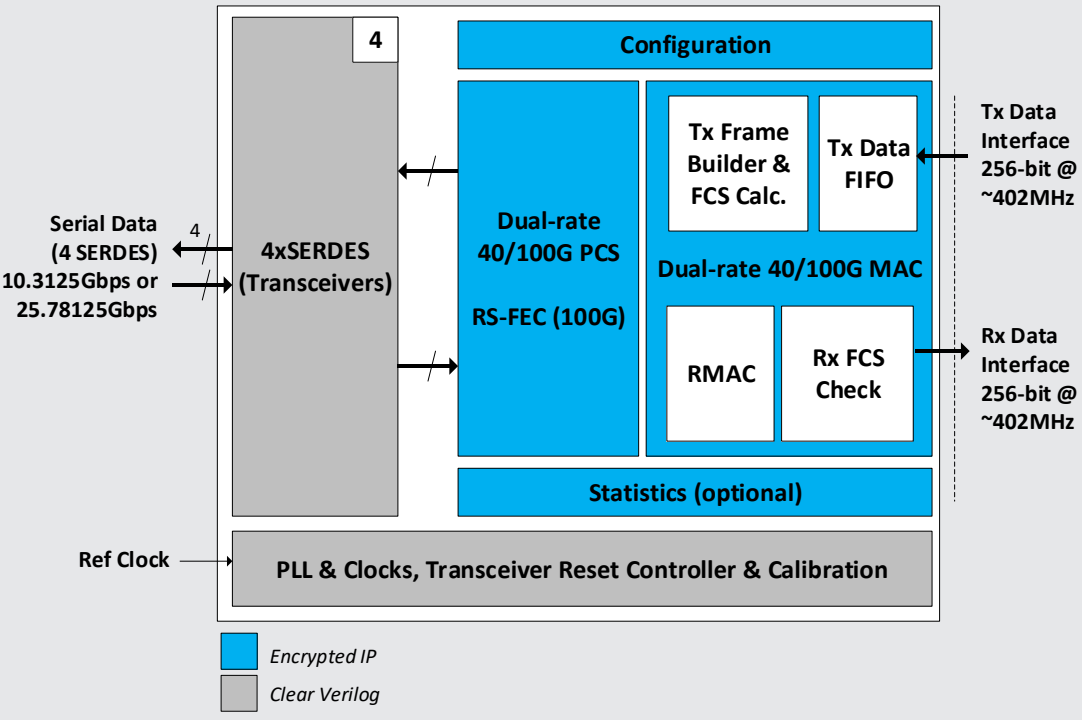
OVERVIEW

The ***40/100G Ethernet MAC & PCS + RS-FEC*** is a multi-rate IP core supporting 40G and 100G line rate. The core is designed using **advanced design techniques** leading to unmatched ultra-low gate count utilization and great latency performances. It includes a **rich set of standard and advanced features** making it ideal for a large number of applications.

The IP core can support full wire line speed with a 64-byte packet length. It also supports back-to-back or mixed length traffic, up to jumbo frame size, with no dropped packets.

The core includes Reed Solomon FEC RS(528, 514, 10) with FEC bypass and error correction bypass capabilities. Two other versions of the IP core are also available, each supporting a single rate, i.e. 40Gbps or 100Gbps (with RS-FEC).

HIGH-LEVEL BLOCK DIAGRAM



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DELIVERABLES

- **Datasheet & user guide**
- **Encrypted Verilog**
- **Constraints file**
- **Reference design**
- **Technical support**
- **Optional Verification IP (UVM based)**
- **Optional IP design customization**

General Features

- Compliant with IEEE802.3-2015 standard
- Ethernet MAC supports 40GbE and 100GbE line rate with flexible feature set
- Soft PCS logic interfacing to standard serial transceiver at 10.3125Gbps and 25.78125Gbps

MAC Features

- Deficit idle counter (DIC) to maintain a 12-byte inter-packet gap (IPG) average
- Programmable IPG length
- Programmable Maximum Receive Unit (MRU), Maximum Transmission Unit (MTU)
- User facing logic interface 256-bit @ ~402.8MHz
- Ethernet flow control and congestion management using pause frames with programmable quanta
- XON / XOFF Frame transmission can be triggered by host (software) interface or directly by core pause frame interface signals
- Programmable Tx minimum packet length with enable/disable padding option
- Programmable Rx minimum packet length
- Tx Frame Check Sequence (FCS) computation and insertion
- Programmable Tx FCS pass-through and corruption insertion modes
- Programmable keep/strip Rx FCS. Programmable Rx FCS error detection and marking
- Programmable Tx and Rx large frame threshold detection
- Programmable Tx and Rx path VLAN detection (Programmable TPID, stacked VLAN)
- Programmable Rx frame discard & marking
- Configurable statistics vector and collector on transmit and receive MAC data

PCS Features

- Supports 40GBASE-R and 100GBASE-R PHY based on 64B/66B encoding with data striping and alignment markers to align data from multiple lanes
- Supports block synchronization and BER monitor
- Supports multiple lanes swapping, lane alignment and deskew
- Configurable statistics vector and collector on transmit and receive PCS

RS-FEC Features

- Built-In Reed Solomon FEC RS(528, 514, 10) with FEC bypass and error correction bypass capabilities
- Statistics information for RS-FEC decoder (FEC align status, corrected & uncorrected FEC codewords)

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ORDERING INFORMATION

- *ENET-100G-R-02 (40/100G + RS-FEC)*

CONTACT

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Performances Overview Example

Multi-Rate 40/100G MAC & PCS + RS-FEC

Device Family [1]	Rate [Gbps]	Resources Utilization [2]			Core clock [MHz]	Wire to Wire Round-Trip Latency [3]
		LUTs	FFs	BRAM		
UltraScale+	40-Gbps	44.2k	43.6k	21	~ 402MHz	315 ns
UltraScale+	100-Gbps (RS-FEC Off)					196 ns
UltraScale+	100-Gbps (RS-FEC On)					399 ns

[1] Other FPGA platforms are also supported. Performances provided for mid speed grade (-2).
[2] Resources utilization includes statistics counters
[3] Latency: Transceiver + PCS + MAC (Tx + Rx)
[4] Contact us for the performance of other product variants